IN THE CLAIMS

Claims 1-17(canceled).

18. (Original) A method of manufacturing a cellular trench-gate semiconductor device comprising active device cells in a cellular area of a semiconductor body, each active device cell having a channel-accommodating region of a second conductivity type between a surface-adjacent source region and an underlying drain region that are of a first conductivity type, the trench-gate being accommodated in an insulated gate trench that extends from the source region through the channel-accommodating region and into the underlying drain region, the trench-gate being dielectrically coupled to the channel-accommodating region by an intermediate gate dielectric layer at sidewalls of the gate trench, wherein a respective end structure is provided for at least one group of the cells by process steps that include:

(a) providing in a portion of the drain region adjacent to a surface of the body a surface-adjacent end region of the second conductivity type that has a higher doping concentration than the channel-accommodating region,

(b) providing a trench-etch mask having windows there-through where the gate trench and an end trench are to be etched into the body, the end trench being an extension of the gate trench into the end region,

(c) etching the gate trench and the end trench into the body,

(d) providing the gate dielectric layer at the sidewalls of the gate trench and end trench, the gate dielectric layer having a smaller thickness than the trench-etch mask,

(e) providing gate material in the gate trench and end trench and extending through the windows in the trench-etch mask and onto an upper surface of the trench-etch mask, and

(f) patterning the gate material by etching away areas thereof to leave the gate material

- in the gate trench to form the trench-gate,
- in the end trench and in the associated window to form an extension of the trench-gate,
- and on an adjacent area of the trench-etch mask to form a conductive layer that is connected to the extension of the trench-gate and that has a lateral extent terminating in an edge on the trench-etch mask.

19. (Currently amended) A method according to Claim 18~~, wherein one or more of the additional device features of Claims 2 to 17 are provided~~.

20. (Currently Amended) A method according to Claim 18 ~~or 19~~, wherein, after patterning the gate material in step (f), the trench-etch mask and its windows are used to provide the source region and/or an insulating capping layer on the trench-gate in a self-aligned manner with respect to the gate trench.

21. (Currently Amended) A method according to Claim 18~~any one of Claims 18 to 20~~, wherein the trench-etch mask comprises silicon nitride that is provided in step (b) over at least a major area of a field-oxide and that protects this field-oxide area during subsequent processing steps such as the steps (c) and (f).

22. (Currently Amended) A method according to Claim 18~~any one of Claims 18 to 21~~, wherein the trench-etch mask comprises

silicon nitride that is provided in step (b), an oxide layer is provided after step (f) over the nitride area of the trench-etch mask in the end structure, and this oxide layer protects the underlying nitride area when the trench-etch mask is subsequently etched away from the active device cells.